

RF SPST Switch Based on Innovative Heterogeneous GaN/SOI Integration Technique

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Abstract — This paper presents an innovative heterogeneous GaN/SOI integration technique implemented on an RF SPST switch. It is intended for 5G applications. The RF switch transistors are GaN based and the substrate is SOI. It allows to integrate RF, analog and digital in one monolithic circuit. The small and large signal measurements show respectively an insertion loss below 0.4 dB up to 30 GHz and a power handling higher than 38 dBm at 900 MHz.

Keywords — Fifth Generation (5G), GaN, SOI, Heterogeneous Integration, RF Switch, Radiofrequency.

I. INTRODUCTION

The radio frequency and microwave industry has made considerable progress in enabling the development of a commercial 5G wireless infrastructure below 6 GHz. The preliminary work on 5G performed in recent years has defined a set of telecommunication standards and scalable architectures to deliver the promised data rate. With the drastic increase of users, Internet of Thing (IoT) devices and Machine to Machine communications, the 4G network will not be able to keep up and will need to evolve. To increase the capacity for the 5G network, two paths are combined: using more bandwidth and deploying antenna arrays. RF architectures for 5G systems are moving towards mMIMO (massive Multi-Inputs Multi-Outputs) systems where beamforming is used to improve the spectral efficiency. By combining these methods the capacity can be increased by up to 20 times in the 3.5 GHz bands (n77, n78) [1].

In addition to higher speeds and greater capacity, the 5G network will need to be extremely energy efficient. In mMIMO systems, the complexity of the system depends on the number of antennas in the array. The processing unit of such a simpler system would consume less energy; however with a smaller number of antennas, the output power becomes a critical performance to achieve. To solve this issue, studies have been conducted to determine what would be the most optimal technology for 5G Front-End modules [2]. According to these studies Gallium Nitride (GaN) seems to be a very good candidate as its power density, power handling and power efficiency are very interesting. In addition to having stable temperature performance [2], GaN has indeed a bandgap of 3.4 eV, several times higher than silicon and electron mobility 1000 times higher than silicon. GaN thus becomes a real competitor to Silicon Germanium (SiGe) or

Silicon Complementary Metal Oxide Semi-conductor (CMOS). The same power can be achieved using 8 to 16 times less MIMO channels than SiGe [2]: resulting into a less complex and more power efficient system.

However despite the great improvement in GaN technology in recent years, it still has significant limitations. GaN technology is not yet mature, available and affordable for high volume production. The power circuitry and logic blocks thus need to be on external chips, typically Silicon based.

In this paper we present SPST (Single Pole Single Throw) switch measurement results using an innovative approach for heterogeneous combination of GaN and Silicon on Insulator (SOI). This heterogeneous integration would enable the combination of RF GaN and Silicon circuitry on the same monolithic chip.

II. ASSEMBLY TECHNIQUE FOR HETEROGENEOUS INTEGRATION

A. State of the Art of Heterogeneous Integration Techniques

The integration of different technologies within a system is the way to obtain the best performances from best-in-class materials for each building block. The most basic technique to integrate several chips of different technology is the Multi-Chip Module (MCM). Due to the inherent large scale of this technique, the interconnections induce parasitic which limits the performances of the overall system. In the context of 5G, where m-MIMO systems are to be used, compactness is required to allow the integration of multiple FEMs as close as possible to their respective antenna.

To decrease the occupied area as well as to lower parasitic elements, many efforts have been put in the development of multi-layer/ multi-chip, wafer-scale and monolithic 3-D heterogeneous integration techniques [3]. Cross-sections of the different techniques are depicted in Fig. 1.

Among the first category of technique, there are the laminated/organic (Fig. 1.a) and Ceramic/Low-Temperature Co-fired Ceramic (LTCC) (Fig. 1.b) substrates. In addition to the multi-technology integration, these techniques permit to lower parasitic elements, allow for additional off-chip routing metal layers and offer high quality factor of passive components such as inductance, transformer and antenna design. These techniques allow shorter interconnections but the integration is not at device level.

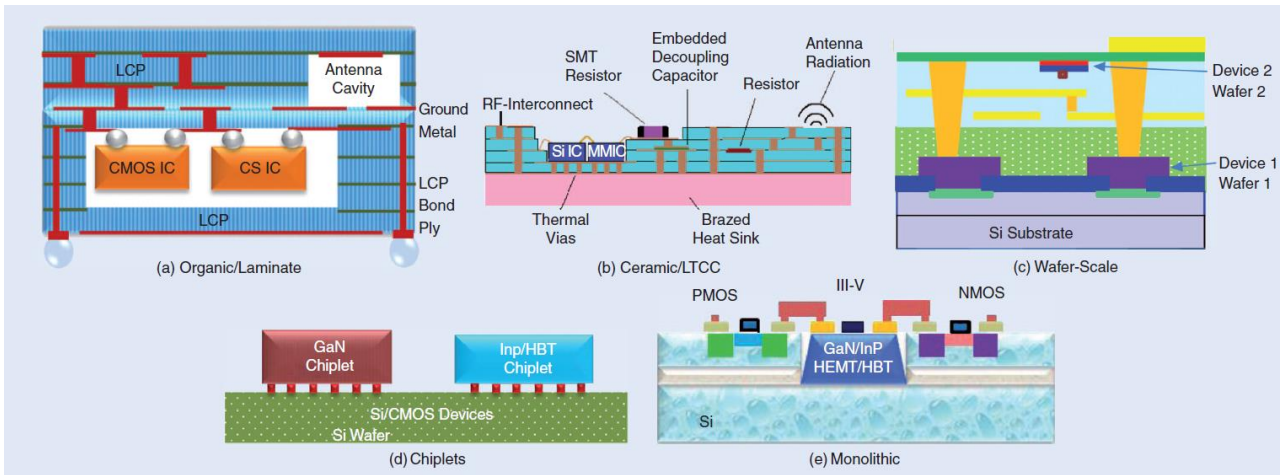


Fig. 1. Schematic cross-sections of (a) Organic/laminate, (b) ceramic/LTCC, (c) wafer-scale, (d) chiplets and (e) monolithic 3-D heterogeneous integration techniques. Figures taken from reference [3].

The monolithic and the wafer-scale 3-D heterogeneous integration techniques allow for the most efficient interconnections between two different technologies. In this category we have the wafer-bonding (Fig. 1.c), the chiplet-based approach (Fig. 1.d) and the monolithic technique (Fig. 1.e). The wafer-bonding consists in bonding together two complete wafers where interconnections are made using Through Silicon Vias (TSV). The chiplet-based approach aims to flip selected chips from one technology onto a wafer of a different technology. Finally, the monolithic technique consists in selective etch on a Si wafer creating a hole where a chosen III-V materials will be grown. These techniques allow the most compact heterogeneous integration in terms of interconnections and occupied area.

B. Innovative 3D Assembly Technique for Heterogeneous GaN/SOI Technology

The proposal of this paper consists in using an advanced 3D packaging technique. Our approach consists in manufacturing separately the GaN and the SOI wafers. Then, we use the concept of chiplet as in Fig. 1.d to place the GaN devices, after removing their native substrate, on the wanted location on the RF-SOI finished 8" wafer. However, unlike Fig. 1.d, the chiplet will be placed face-up on top of the SOI wafer. To connect the GaN chiplet to the SOI components, a Re-Distribution Layer (RDL), which is a post-processed copper metal layer, is deposited above the last layer of both SOI and GaN technologies (see Fig. 2).

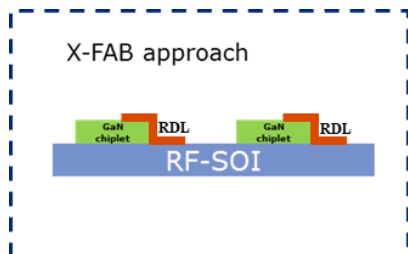


Fig. 2. X-FAB 3D packaging technique proposal

This technique pushes the integration to transistor level as the dimension of the chiplet could be scaled down to few tens of micrometers (see Fig. 3). Thus, we are considering it as a monolithic integration just like the Fig. 1.e approach.

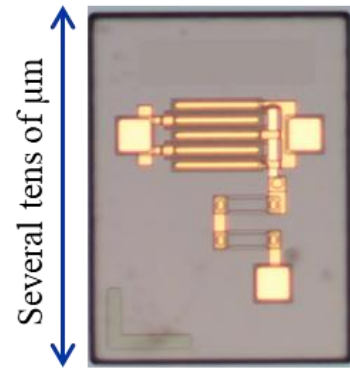


Fig. 3. Picture of one chiplet

III. ADVANTAGES OF THE HETEROGENEOUS TECHNOLOGY FOR SWITCH APPLICATION

This heterogeneous technology consists in having a monolithic circuit, resulting in a smaller, cheaper and less complex circuitry than a system in package or a multi-chip module. It also helps getting a better control over parasitic elements and performances as we are pushing the integration into device level. Furthermore, this innovative integration technique combines the best of both GaN and SOI technologies. It allows to:

- benefit from the integration capabilities of CMOS,
- overcome the availability and the maturity of GaN,
- reduce the cost of the final circuit, as only few devices are used where needed,
- benefit from the high power capability of the GaN.

For example, an RF switch circuit typically needs control logic, IO interface and negative voltage generator in addition to the RF switching element (see Fig. 4). GaAs, GaN, and PIN diode switches require in general separate CMOS die for

interface, negative voltage generator, and control logic. This constraint can be so avoided using the GaN on SOI approach as it allows having a monolithic circuit.

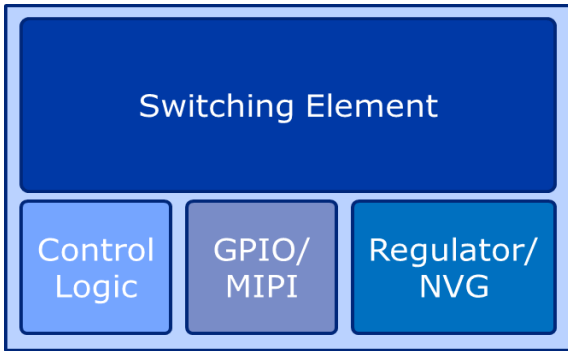


Fig. 4. Block diagram of a complete switch circuit

In addition to area saving, this heterogeneous integration improves GaN transistor intrinsic performances. The vertical isolation of the GaN on Si technology is poor compared to typical technologies used for switch applications such as SOI technology. Some process techniques are developed to improve this isolation but they remain insufficient. By removing the substrate the vertical leakage is expected to be significantly reduced resulting in improved HEMT voltage breakdown [4].

IV. MEASUREMENT SETUP AND RESULTS

A. Circuit topology

To validate our integration concept, a SPST switch has been designed for on-wafer small and large signal characterizations (see Fig. 5). It is composed of two GaN transistors in series on a SOI substrate. Integrated drain-source resistors are present as well as a gate resistor to make the gate floating.

This Device Under Test (DUT) is intended to be characterized on wafer. The GaN chiplet is connected to the Ground-Signal-Ground (GSG) pads on the SOI wafer using the RDL. A DC pad is added to bias the gate.

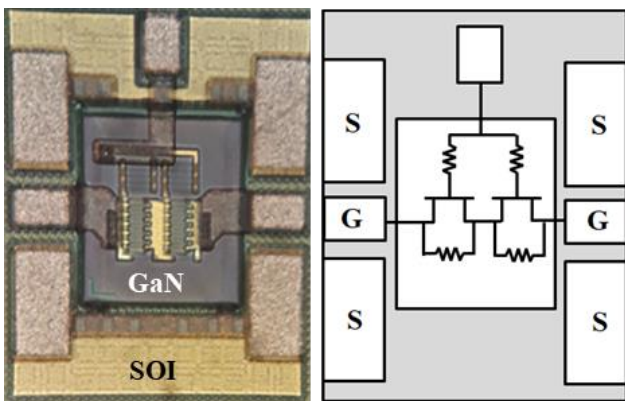


Fig. 5. Photograph (Left) and schematic (Right) of the RF GaN switch on SOI

B. Small signal characterization

The small signal characterization of this heterogeneous device is performed from 0.2 to 30 GHz on wafer with a Vector Network Analyser (VNA). The reference planes of the measurement are at the tips of the probes. Then, the measurements results are de-embedded using the open and short structures shown in Fig. 6 to be in the transistor plane.

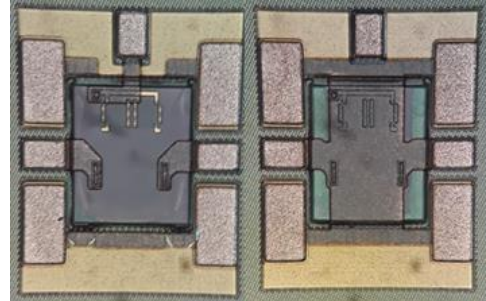


Fig. 6. Photograph of the open (Left) and the short (Right) used to de-embed the RF GaN on SOI switch measurements

To evaluate the performances of this heterogeneous GaN/SOI switch, its measurements were compared to the simulation of its equivalent in GaN on Si. The reason behind this choice is the unavailability of GaN on Si equivalent structures. Nevertheless, previous characterization campaigns showed a good fit between simulation and experimental results.

The insertion loss comparison is shown in Fig. 7. The heterogeneous structure presents lower insertion loss than the simulated GaN on Si switch, especially at high frequencies. This difference reaches indeed more than 1 dB at 30 GHz. Another interesting feature is that the insertion loss is flatter in measurement in the 0.2 – 30 GHz frequency band compared to the simulation. This behaviour confirms the reduction of the vertical capacitive coupling to the substrate.

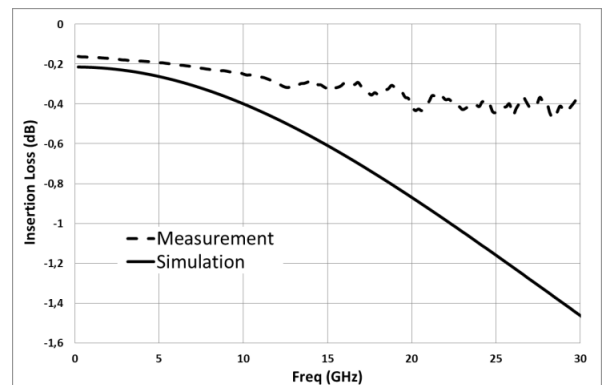


Fig. 7. Insertion loss comparison of the measured heterogeneous SPST (dashed line) and the simulated GaN on Si structure (solid line)

Fig. 8 shows the isolation comparison of the measured heterogeneous GaN/SOI structure and the simulated GaN on Si switch. The results show similar behaviour. We can still observe a small difference in isolation level of starting from 5 GHz.

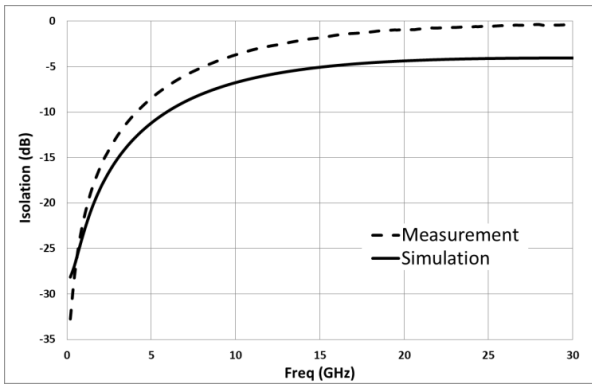


Fig. 8. Isolation comparison of the measured heterogeneous SPST (dashed line) and the simulated GaN on Si structure (solid line)

Both of these plots show that this heterogeneous integration technique demonstrates similar small signal results compared to GaN on Si up to 3 GHz and much lower insertion loss at high frequency (>1 dB @ 30 GHz). Given the low insertion loss of the heterogeneous SPST, it could be resized to improve the isolation.

C. Large signal characterization

The large signal characterization of this heterogeneous device is performed at 900 MHz with an input power sweeping from 0 to 38 dBm. The continuous wave (CW) input signal is generated by a synthesizer, amplified by a power amplifier stage and filtered by a narrow band filter with 100 dB rejection. Thus, no harmonic components are injected in the DUT. At the output of the DUT, the signal is split into fundamental output power (Pout), second harmonic (H2) and third harmonic (H3) using three different filters centred to the three respective frequencies. The noise floor of the measurement setup is around -100 dBm.

The large signal measurement results are illustrated in Fig. 9 and Fig. 10. These results show that the DUT does not present any compression up to 38 dBm as seen in the large signal insertion loss and Pout curves (see Fig. 9). The measurement uncertainties are estimated to ± 0.1 dB. The H2 and H3 present 68 dBc and 75 dBc respectively at 38 dBm (see Fig. 10).

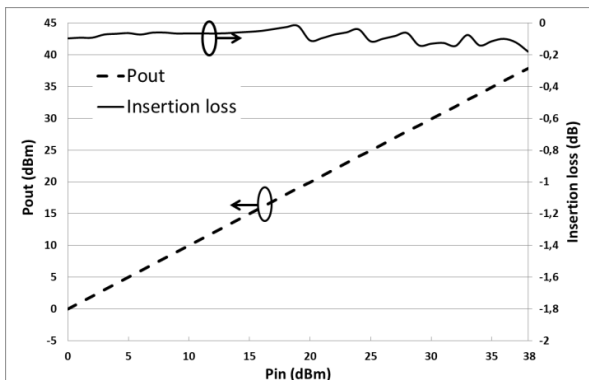


Fig. 9. Pout (dashed line) and insertion loss (solid line) as a function of the input power (Pin)

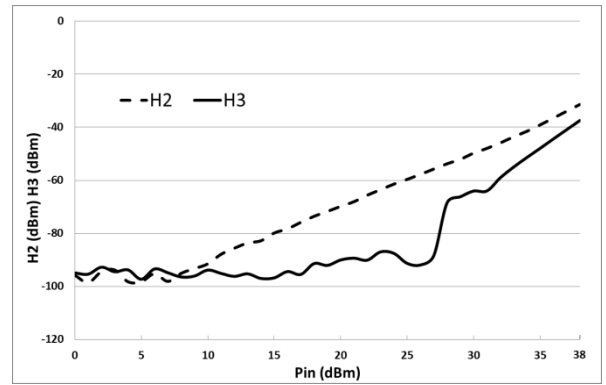


Fig. 10. Power of H2 (dashed line) and H3 (solid line) as a function of the input power (Pin)

V. CONCLUSION

In this paper, we have presented the first small and large signal characterization of an heterogeneous GaN/SOI RF switch. To our knowledge, this is the first time that this monolithic heterogeneous integration technique is used for RF applications. This approach allows to integrate several functionalities in the same circuit.

To validate this concept, samples were built and characterized on-wafer. Overall, the preliminary results are encouraging in both small and large signals. The DUT showed insertion loss below 0.4 dB from DC to 30 GHz. The breakdown of the DUT is beyond 38 dBm which is the maximal achievable power with our current characterization bench. Characterizations at higher power are planned to determine the maximal power handling of this DUT. Moreover, a study for thermal dissipation is currently ongoing for this innovative technique. Our first characterizations show that the heat dissipation looks sufficient for low insertion loss switch applications.

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